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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,336	KELLER ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20 February 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 32-68 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Preliminary Amendment and Information Disclosure Statement as received on 2/20/04.

Continued Examination

3. This application repeats a substantial portion of prior Application No.09418097, filed October 14, 1999, and adds and claims additional disclosure not presented in the prior application. More specifically, the claims now include language regarding each field of each line predictor entry being fixedly assigned to a respective decoder of a plurality of decoders by the physical position of the field within the entry and independent of the fetch address. The original specification only discloses that field 108 is coupled only to decoder 24D. There is no original disclosure regarding fields 102, 104, and 106 each being coupled to a respective decoder. And, the labels in the fields in Fig.6 do not support the claim language as they are just labels with no description in the specification. Consequently, since this application names an inventor or inventors named in the prior application, the examiner believes and now assumes that applicant meant to file a continuation-in-part of the prior application as opposed to a continuation of the prior application. The beginning of the specification should be changed to reflect this.

Oath/Declaration

4. A newly executed oath or declaration must be filed in any continuation-in-part application, which application may name all, more, or fewer than all of the inventors named in the prior application. See 37 CFR 1.63(e).

Information Disclosure Statement

5. Regarding the cited foreign patent documents, applicant has cited document number 93/17385 twice, both having different dates. The examiner has confirmed that this document was indeed published in September 2003. Consequently, the incorrect citation is not considered and crossed out by the examiner.

Specification

6. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The specification does not support the language in the claims regarding each field of each line predictor entry being fixedly assigned to a respective decoder of a plurality of decoders by the physical position of the field within the entry and independent of the fetch address. The specification only discloses that field 108 is coupled only to decoder 24D. There is no disclosure about fields 102, 104, and 106 each being coupled to a respective decoder. And, the labels in the fields in Fig.6 do not support the claim language as they are just labels with no description in the specification.

Drawings

7. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, each field of each line predictor entry being fixedly assigned to a respective decoder of a plurality of decoders by the physical position of the field within the entry and independent of the fetch address must be shown or the feature(s) canceled from the claim(s). That is, there is no Figure which shows or supports fields being fixedly coupled to respective decoders based on physical position and independent of the fetch address. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 32-68 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. More specifically, the independent claims each include language regarding each field of each line predictor entry being fixedly assigned to a respective decoder of a plurality of decoders by the physical position of the field within the entry and independent of the fetch address. However, applicant has not claimed how such an assignment occurs. Assuming four fields, as shown in applicant's Fig.6, if four decoders exist, each of the fields may be coupled to the same decoder. Or, two fields may be coupled to one decoder while the other two fields are coupled to another decoder. Or, as another example, each field may be coupled to a single, different decoder (a 1-to-1 decoder-to-field correspondence). As can be seen, the claim language allows for multiple interpretations, none of which has been enabled by applicant. This enablement is essential because each interpretation would require different circuitry and possibly timing, wherein the circuitry and timing may be more complicated in one interpretation of the claim). And, without knowing how the circuitry and timing are implemented, the overall operation of the processor is unknown.

10. Claim 57 recites the limitation "The method as recited in claim 48". There is insufficient antecedent basis for this limitation in the claim. For purposes of this examination, the examiner will assume claim 57 is dependent on claim 49.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Assuming a continuation-in-part application, claims 32, 33, 37, 49-50, and 60-61 are rejected under 35 U.S.C. 102(b) as being anticipated by Ginosar et al., U.S. Patent No. 5,978,899 (herein referred to as Ginosar).

13. Referring to claim 32, Ginosar has taught a processor comprising:

a) a plurality of decoders configured to decode instructions. See Fig.2, components 30.

b) an alignment unit coupled to the plurality of decoders and to receive a plurality of instruction bytes fetched from a location identified by a fetch address and configured to align instructions within the plurality of instruction bytes to the plurality of decoders. See Fig.2, components 28, and column 6, lines 47-67. Note that components 28 (collectively referred to as the alignment unit) receive the instruction bytes from buffer 26 in response to a fetch address, and align the instruction bytes to the decoders.

c) a line predictor (Fig.1 and Fig.2, components 10, 12, and 26) coupled to receive the fetch address and coupled to the alignment unit (Fig.2, components 28), the line predictor including a

first memory (Fig.2, component 26) comprising a plurality of entries (column 6, lines 52-54), wherein each entry of the plurality of entries comprises a plurality of fields (see Fig.2 and column 6, lines 49-64, and note that the entry is divided into byte fields), and wherein each field of the plurality of fields is fixedly assigned to a respective decoder of the plurality of decoders by the physical position of the field within the entry and independent of the fetch address (see Fig.2, and note that the byte from the column i field is sent to the decoder in column i, whereas, the byte from the column i+1 field is sent to the decoder in column i+1, and so on), and wherein the line predictor is configured to select a first entry of the plurality of entries, the first entry corresponding to the fetch address (clearly the instruction line being decoded corresponds to a fetch address), and wherein each field of the plurality of fields in the first entry includes a respective instruction pointer of a first plurality of instruction pointers stored in the first entry, and wherein the respective instruction pointer, if valid, locates an instruction within the plurality of instruction bytes fetched from the location identified by the fetch address, and wherein the alignment unit is configured to align the instruction located by the respective instruction pointer to the respective decoder due to the respective instruction pointer being included in the field assigned to the respective decoder. Note from column 5, lines 48-51, that instructions may be one byte to a maximum number of bytes. Consequently, a byte which represents an instruction in column i will be aligned by component 28 in column i with the decoder 30 in column i.

14. Referring to claim 33, Ginosar has taught a processor as described in claim 32. Ginosar has further taught that the first entry is further configured to store a next entry indication identifying a second entry of the plurality of entries within the first memory, wherein the line predictor is configured to subsequently select the second entry to provide a second plurality of

instruction pointers stored therein responsive to the next entry indication. See column 6, lines 52-57 and note that the buffer is implemented as a FIFO. Consequently, it inherently must track which entry is next to be outputted.

15. Referring to claim 37, Ginosar has taught a processor as described in claim 32. Ginosar has further taught that the first entry is further configured to store control information corresponding to the instructions located by the first plurality of instruction pointers. The bytes themselves are control information as they will dictate what operations the system performs, and the bytes are used in determining the length of the instructions. See the abstract.

16. Referring to claim 49, it has been noted by the examiner that the processor of claim 32 performs the method of claim 49. Consequently, claim 49 is rejected for the same reasons set forth in the rejection of claim 32 above.

17. Referring to claim 50, it has been noted by the examiner that the processor of claim 33 performs the method of claim 50. Consequently, claim 50 is rejected for the same reasons set forth in the rejection of claim 33 above.

18. Referring to claim 60, it has been noted by the examiner that the processor of claim 32 includes the line predictor of claim 60. Consequently, claim 60 is rejected for the same reasons set forth in the rejection of claim 32 above.

19. Referring to claim 61, it has been noted by the examiner that the processor of claim 33 includes the line predictor claim 61. Consequently, claim 61 is rejected for the same reasons set forth in the rejection of claim 33 above.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 41-42 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ginosar, as applied above, in view of Nanda et al., U.S. Patent No. 5,329,627 (as disclosed by applicant and herein referred to as Nanda).

22. Referring to claim 41, Ginosar has taught a processor as described in claim 37.

a) Ginosar has further taught an instruction cache configured to store instruction bytes. See Fig.1, component 10.

b) Ginosar has not explicitly taught a translation lookaside buffer (TLB) coupled to said instruction cache and configured to translate virtual addresses to physical addresses wherein said fetch address is a virtual address, and wherein said TLB is configured to translate said fetch address to a corresponding physical address and to provide said corresponding physical address to said instruction cache to fetch said plurality of instruction bytes. However, Nanda has taught the use of a TLB in order to translate virtual addresses into physical addresses. See column 1, lines 41-52. It is well known in the art that physical addresses are used in exchanges between the CPU and memory components such as cache or main memory. In fact, each physical address uniquely identifies each memory location within the memory space. Any other address must be translated in order to access the correct memory location. A person of ordinary skill in the art would have recognized the advantage of using a translation lookaside buffer for such translation.

One of the advantages is the elimination of time spent in translating the addresses each time. Instead, it is well known in the art that the address mappings could be stored in the TLB for quick reference. Therefore, in order to improve the efficiency of the overall system, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a TLB in the system of Ginosar as taught by Nanda in order to translate the virtual address into a physical address for memory access.

23. Referring to claim 42, Ginosar in view of Nanda has taught a processor as described in claim 41. Ginosar in view of Nanda has not taught that the virtual address comprises a linear address. However, Official Notice is taken that x86 variable-length instructions are well known in the art. And, since they are well know, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement such an instruction set into the system of Ginosar. Furthermore, it has been noted that the applicant has disclosed (on page 26, lines 27-29, and on page 27, lines 1-2) that within the x86 architecture, virtual addresses may be linear addresses generated according to a segmentation mechanism. Since, Ginosar's system would employ the x86 architecture, it follows that a virtual address comprises a linear address.

24. Referring to claim 57, it has been noted by the examiner that the processor of claim 41 performs the method of claim 57. Consequently, claim 57 is rejected for the same reasons set forth in the rejection of claim 41 above.

25. Claims 58-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ginosar, as applied above.

26. Referring to claim 58, it has been noted that the processor of claim 58 is the same as the processor of claim 32. Consequently, claim 58 is rejected for the same reasons set forth in the rejection of claim 32. In addition, although Ginosar has not explicitly taught an input/output (I/O) device configured to communicate between said computer system and another computer system to which said I/O device is couplable, Official Notice is taken that modems are well known and expected devices in the art which allow two or more processors to communicate with one another. As a result, in order to allow for communication between processors, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ginosar to include a modem that is coupled to the processor.

27. Referring to claim 59, Ginosar has taught a processor as described in claim 58. Furthermore, Ginosar has taught that the I/O device comprises a modem. See the rejection of claim 58 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
October 7, 2004

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